IN THE CLAIMS

For the convenience of the Examiner, all pending claims of the present Application are shown below in numerical order whether or not an amendment has been made and applying the revised format guidelines of 37 CFR 1.121.

1. (Currently Amended) A network interface card, comprising:

a first printed circuit board;

first and second connectors coupled with the first printed circuit board;

a plurality of ethernet communication paths forming at least a portion of a communication coupling between the first and second connectors;

the first connector configured to receive a third connector associated with a midplane;

a chip coupled with the first printed circuit board wherein the plurality of ethernet communications paths couple the first connector with the chip;

a first communication link coupling the chip and the second connector;

wherein the chip consolidates data received through the first connector for distribution of the data to the second connector;

a single board computer coupled with the first printed circuit board; and

a second communication link coupling the chip with the single board computer.

2. (Currently Amended) The network interface card of Claim 1, further comprising:

a ~~third~~ fourth connector coupled with the first printed circuit board; and

wherein the plurality of ethernet paths form at least a portion of the coupling between the ~~third~~ fourth connector and the chip.

3. (Currently Amended) The network interface card of Claim 1, further comprising:

a ~~third~~ fourth connector coupled with the single board computer; and

wherein the ~~third~~ fourth connector is operable to distribute data between the single board computer and a management network.

4. (Currently Amended) The network interface card of Claim 1, further comprising a ~~third~~ fourth connector forming the coupling between the single board computer and the second communication link.

5. (Original) The network interface card of Claim 1, wherein the single board computer comprises:

a second printed circuit board coupled with the first printed circuit board;

a central processing unit coupled with the second printed circuit board; and

memory integrated circuits coupled with the second printed circuit board.

6. (Original) The network interface card of Claim 1, wherein the chip includes a repeater chip.

7. (Original) The network interface card of Claim 1, wherein the chip includes a switch chip.

8. (Original) The network interface card of Claim 2, wherein the third connector includes a gigabit ethernet connector.

9. (Original) The network interface card of Claim 2, wherein the third connector includes a gigabit interface connector (GBIC).

10. (Currently Amended) A network interface card, comprising:

a first printed circuit board;

a chip coupled with the first printed circuit board;

first and second connectors coupled with the first printed circuit board, each of the first and second connectors ~~adapted~~ configured to receive a plurality of first ethernet communications links, through a midplane associated with a plurality of web server processing cards;

a plurality of second ethernet communications links coupling the first connector and the chip;

a plurality of third ethernet communications links coupling the second connector and the chip;

a high density communication path coupling the chip with a third connector; and

wherein the chip is operable to distribute data communications between one of the first and second connectors, and the third connector.

11. (Original) The network interface card of Claim 10, wherein the chip includes a repeater chip.

12. (Original) The network interface card of Claim 10, wherein the chip includes a switch chip.

13. (Original) The network interface card of Claim 11, wherein the repeater chip includes an integrated network hub and the repeater chip is operable to aggregate all 10/100/1000 megabits per second ethernet communications received through the first and second connectors.

14. (Original) The network interface card of Claim 13, wherein the integrated network hub includes a repeater chip having at least ten ports.

15. (Original) The network interface card of Claim 12, wherein the switch chip includes an integrated network switch and the switch chip is operable to aggregate all 10/100/1000 megabits per second ethernet communications received through the first and second connectors.

16. (Original) The network interface card of Claim 15, wherein the integrated network switch includes a switch chip having at least ten ports.

17. (Original) The network interface card of Claim 10, further comprising:

a fourth connector coupled with the first printed circuit board;

a second high density communication path coupling the repeater chip with the fourth connector; and

wherein the second high density communication path and the fourth connector provide at least a portion of a redundant communication path between the chip and a network router.

18. (Original) The network interface card of Claim 10, further comprising:

a fourth connector coupled with the first printed circuit board;

a second high density communication path coupling the repeater chip with the fourth connector; and

wherein the fourth connector is operable to receive a fifth connector associated with a second network interface card.

19. (Original) The network interface card of Claim 10, wherein the third connector includes an RJ-21 connector adapted to receive a fourth connector associated with a network router.

20. (Original) The network interface card of Claim 12, wherein the switch chip includes a multiple port 10 100 Base T switch having fiber gigabit uplinks.

21. (Original) The network interface card of Claim 12, wherein the switch chip includes a multiple port 10/100 Base T switch having copper gigabit uplinks.

22. (Original) The network interface card of Claim 12, wherein the switch chip is operable to address and distribute messages according to packet headers including port addresses associated with network components.

23. (Original) The network interface card of Claim 10, wherein the first connector includes a built-in serial port.

24. (Original) The network interface card of Claim 10, further comprising:

a single board computer coupled with the first printed circuit board; and

a second high density communication path coupling the chip with the single board computer.

25. (Original) The network interface card of Claim 24, wherein the single board computer comprises:

a second printed circuit board coupled with the first printed circuit board;

a central processing unit coupled with the second printed circuit board; and

memory integrated circuits coupled with the second printed circuit board.

26. (Cancelled)

27. (Cancelled)

28. (Cancelled)

29. (Cancelled)

30. (Cancelled)

31. (Cancelled)

32. (Cancelled)

33. (Cancelled)

34. (New) The network interface card of Claim 1, wherein the information received by the single board computer comprises telemetry data.

35. (New) The network interface card of Claim 1, wherein the single board computer communicates with the management network in response to received information indicating that a first computer communicating with the midplane has exceeded a set temperature.

36. (New) The network interface card of Claim 1, wherein the single board computer communicates with the management network by instructing a first component of the management network to replicate the data of a second component of the management network.

37 (New) The network interface card of Claim 1, wherein the single board computer communicates with the management network by instructing a first component of the management network to assume the operations of a second component of the management network.

38. (New) The network interface card of Claim 1, wherein the first and second connectors comprise first and second high density connectors, the first and second connectors each operable to receive traffic from a plurality of web servers.

39. (New) A network interface card, comprising:

a first printed circuit board;

a chip coupled with the first printed circuit board;

first and second connectors coupled with the first printed circuit board, each of the first and second connectors configured to receive a plurality of first ethernet communications links, through a midplane associated with a plurality of web server processing cards;

a plurality of second ethernet communications links coupling the first connector and the chip;

a plurality of third ethernet communications links coupling the second connector and the chip;

a high density communication path coupling the chip with a third connector, the chip operable to distribute data communications between one of the first and second connectors, and the third connector, the third connector operable to communicate data communications to a management network; and

a communication path coupling the chip with a fourth connector, the chip operable to distribute data communications between one of the first and second connectors and the fourth connector, the fourth connector operable to communicate data communications to an Internet.